CLAIMS

1. An apparatus for variably scaling video picture signals comprising:

a first circuit configured to generate one or more data signals vertically scaled to a first value in response to (i) said video picture signals and (ii) one or more control signals; and

a second circuit configured to generate one or more output signals horizontally scaled to a second value in response to (i) said one or more data signals and (ii) said one or more control signals, wherein said first value and said second value are independently selectable.

2. The apparatus according to claim 1, wherein said first circuit comprises (i) a luma circuit configured to generate a luma component of said output signals and (ii) a chroma circuit configured to generate one or more chroma components of said output signals.

3. The apparatus according to claim 1, wherein said second circuit is further configured to decimate and interpolate said data signals.

4. The apparatus according to claim 1, wherein said apparatus is programmable to scale said output signals to one or more display modes.

5. The apparatus according to claim 4, wherein said apparatus is configured to automatically reset a starting address

of a display line when an end of said display line is not displayed.

6.   The apparatus according to claim 4, wherein said one or more display modes are in a range of 0.25 times to 4.0 times said video picture signals.

7.   The apparatus according to claim 2, wherein said luma circuit comprises:
a first memory circuit configured to buffer said video picture signals;
a first filter circuit serially coupled to said first memory circuit and configured to generate said luma component; and
a second memory circuit serially coupled to said first filter circuit and configured to buffer said data signals.

8.   The apparatus according to claim 7, wherein said chroma circuit comprises:
a third memory circuit configured to buffer said video picture signals;
a second filter circuit serially coupled to said third memory circuit and configured to generate said one or more chroma components; and
a fourth memory circuit serially coupled to said second filter circuit and configured to buffer said data signals.

9.   The apparatus according to claim 1, wherein said first circuit comprises a generator circuit, wherein said generator

circuit is configured to generate said control signals in response to a microcontroller circuit.

10. The apparatus according to claim 9, wherein said apparatus comprises a single-chip MPEG-2 decoder.

11. The apparatus according to claim 8, wherein said first filter circuit further comprises one or more first accumulator circuits configured to define a number of said video picture signals to be buffered in said first memory circuit in response to said one or more control signals.

12. The apparatus according to claim 11, wherein said second filter circuit further comprises one or more second accumulator circuits configured to define a number of said video picture signals to be buffered in said third memory circuit in response to said one or more control signals.

13. The apparatus according to claim 1, wherein said second circuit controls an output rate of said data signals from said first circuit in response to said first value and said second value.

14. The apparatus according to claim 12, wherein said second circuit comprises one or more third accumulator circuits configured to select one or more of said data signals in response to said one or more control signals.

15. An apparatus for variably scaling video picture signals comprising:

means for generating one or more data signals vertically scaled to a first value in response to (i) said video picture signals and (ii) one or more control signals; and
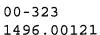
means for generating one or more output signals horizontally scaled to a second value in response to (i) said one or more data signals and (ii) said one or more control signals, wherein said first value and said second value are independently selectable.

16. A method for variably scaling video picture signals comprising the steps of:

(A) generating one or more data signals vertically scaled to a first value in response to (i) said video picture signals and (ii) one or more control signals; and

(B) generating one or more output signals horizontally scaled to a second value in response to (i) said one or more data signals and (ii) said one or more control signals, wherein said first value and said second value are independently selectable.

17. The method according to claim 16, wherein step B further comprises the steps of:

decimating said data signals; and

interpolating said data signals.

18. The method according to claim 16, wherein step B further comprises the step of:

controlling an output rate of said data signals from said first circuit in response to said first value and said second value.

19. The method according to claim 16, wherein said method further comprises the step of:

programmably scaling said output signals to one or more display modes.

20. The method according to claim 19, wherein said step further comprises the step of:

automatically resetting a display line address when some of a picture is not displayed.

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